

ABSTRACT

An application specific integrated circuit (ASIC) is disclosed. The ASIC comprises a standard cell, the standard cell including a plurality of logic functions. The ASIC further includes at least one FPGA interconnect coupled to at least a portion of the logic functions.

5 The FPGA interconnect can be configured to select a particular logic function of the plurality of logic functions. An ASIC in accordance with the present invention allows “field selection” of functions that are connected to the internal bus(es) and to external I/O. In addition, functional block connections made with internal buses can be significantly wider and faster than buses brought on chip via external chip I/Os. Further, the ASIC reduces cost because selective bus connections can be made internal to the chip, thus eliminating the need for external pins. Finally, the ASIC reduces the cost of the packaged component by allowing the chip to be packaged in a lower pin count package.

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